



Title of Invention: A Simple and Effective Solution to Rectifier Recovery Problems
 Inventors Name: LEE, F. ET AL.
 Docket No./Application No.: 09/843,143

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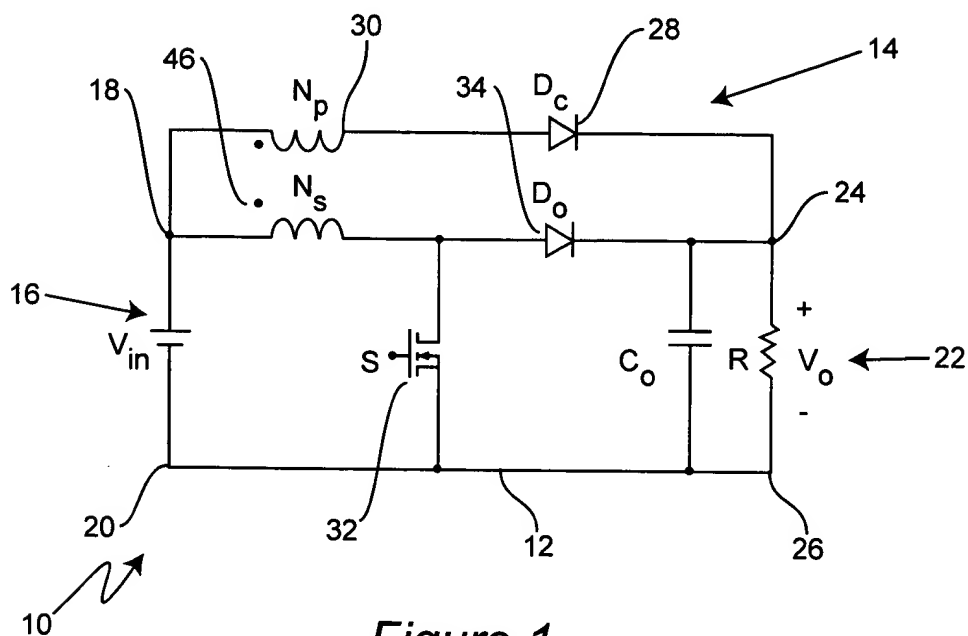


Figure 1

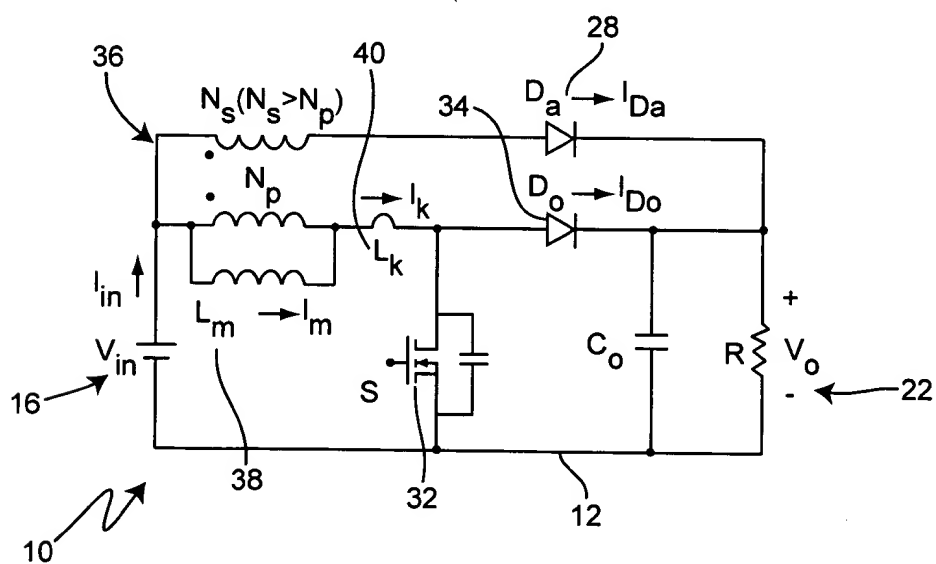


Figure 2



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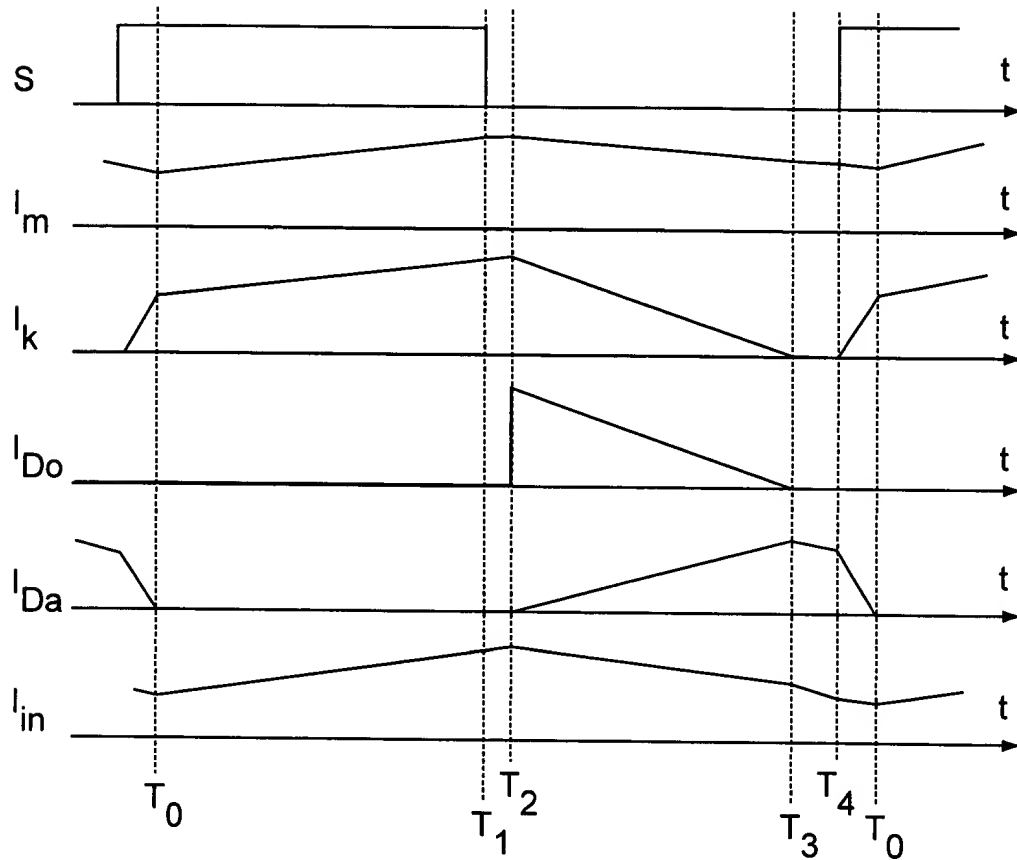


Figure 3



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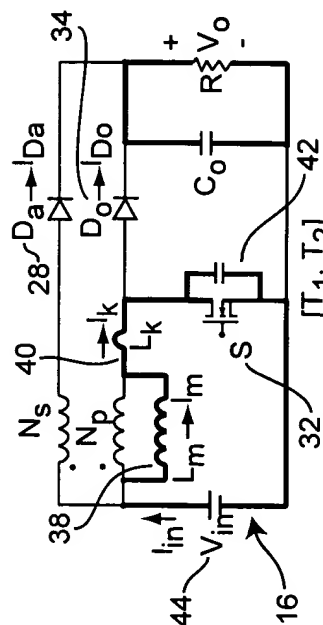


Figure 4B

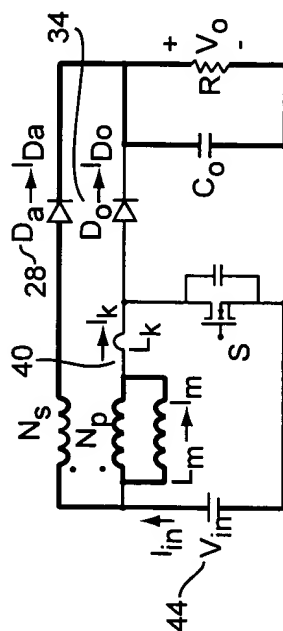


Figure 4D

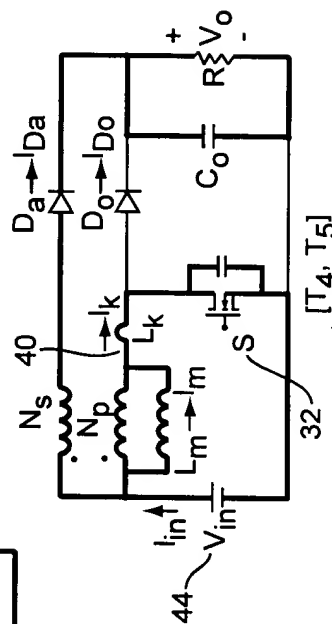


Figure 4E

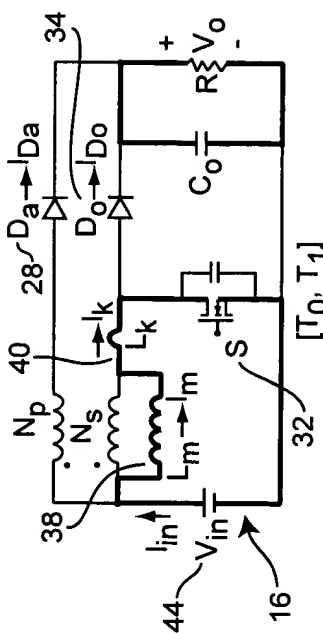


Figure 4A

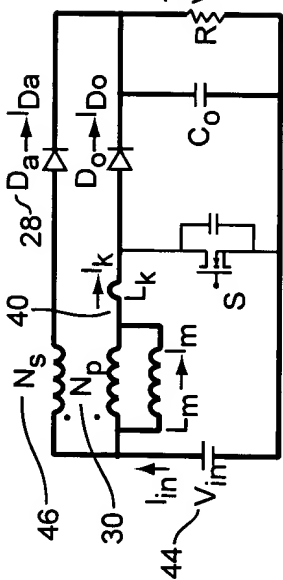


Figure 4C



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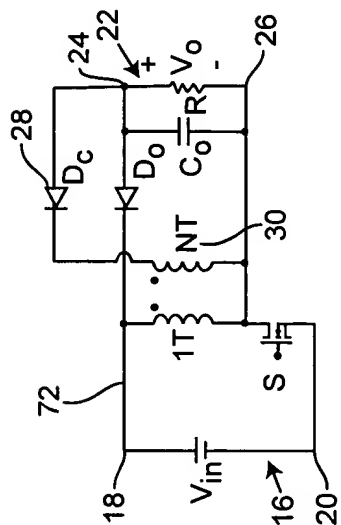


Figure 5C

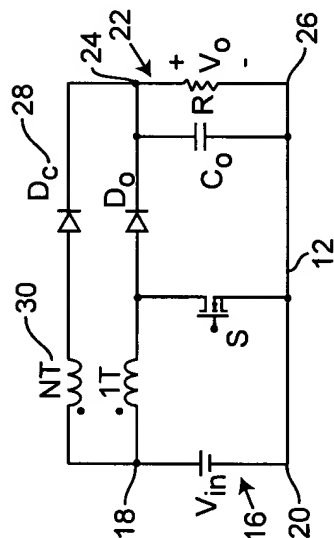


Figure 5B

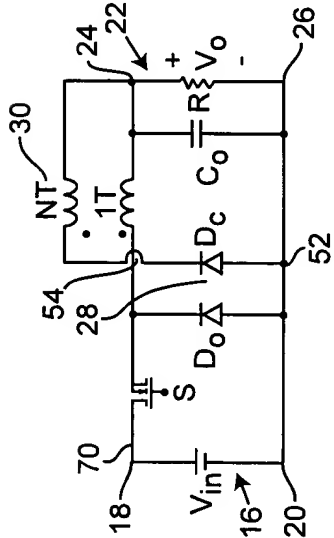


Figure 5A

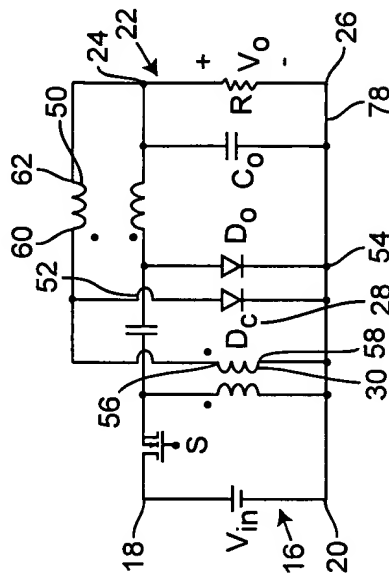


Figure 5F

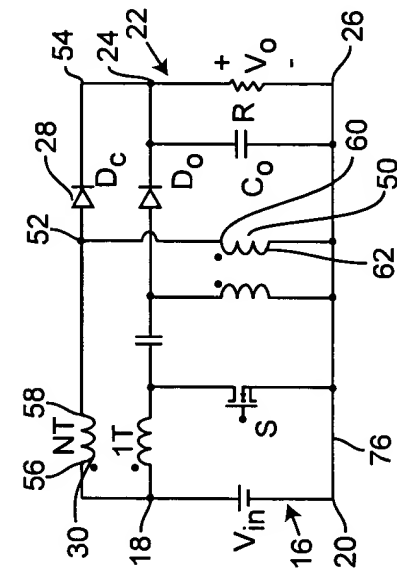


Figure 5E

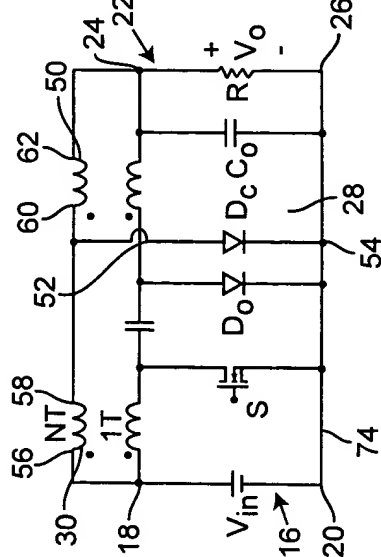


Figure 5D



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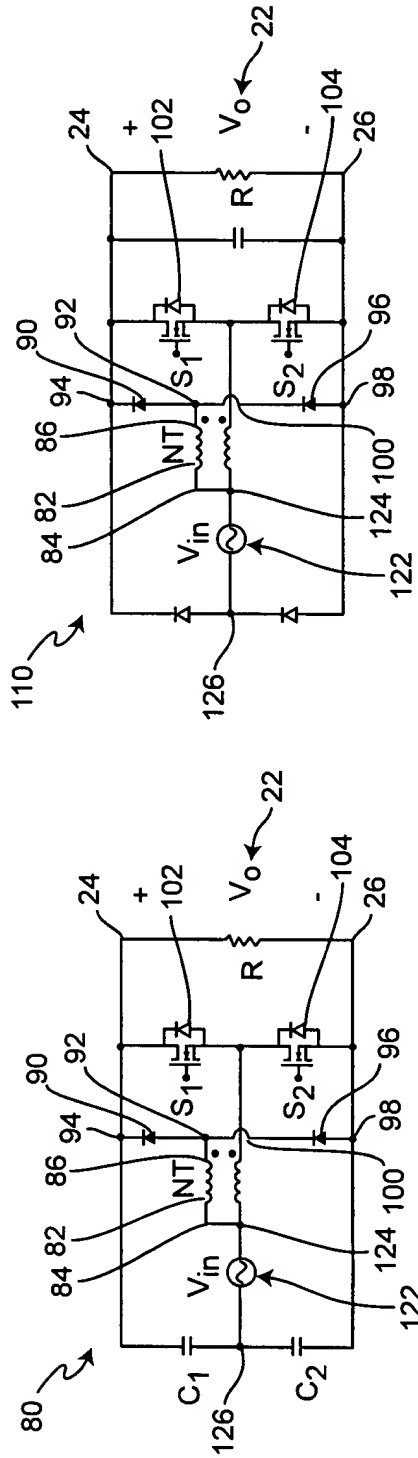


Figure 6B

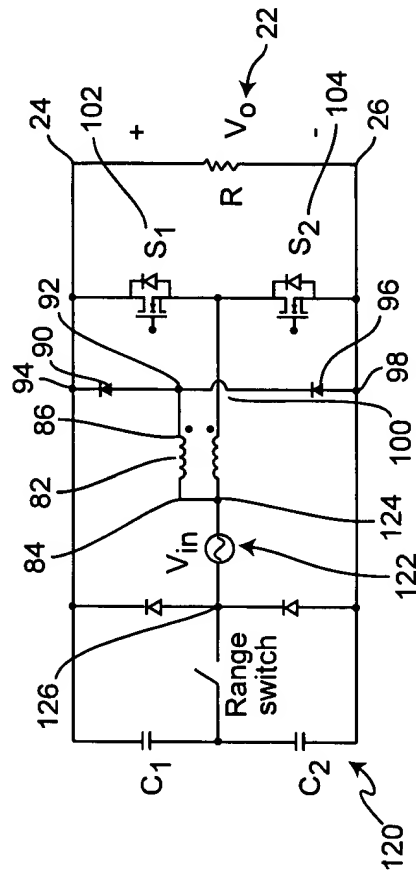


Figure 6C



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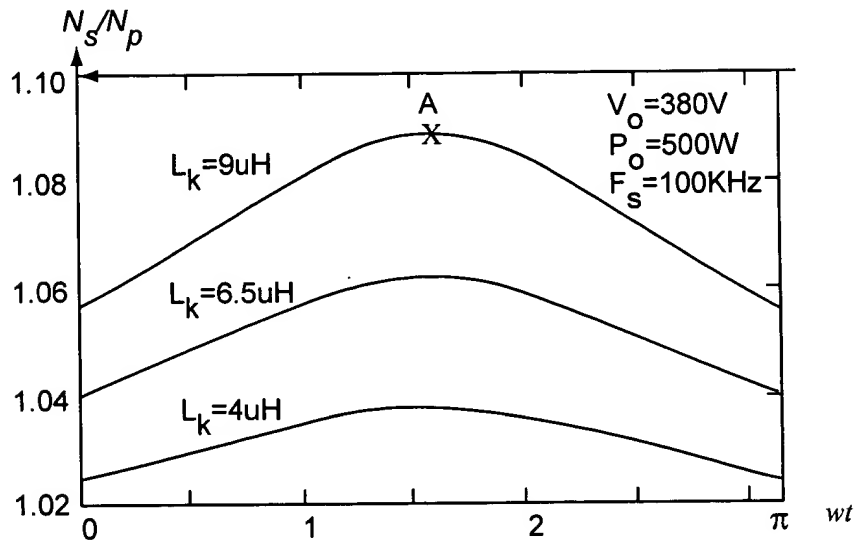


Figure 7

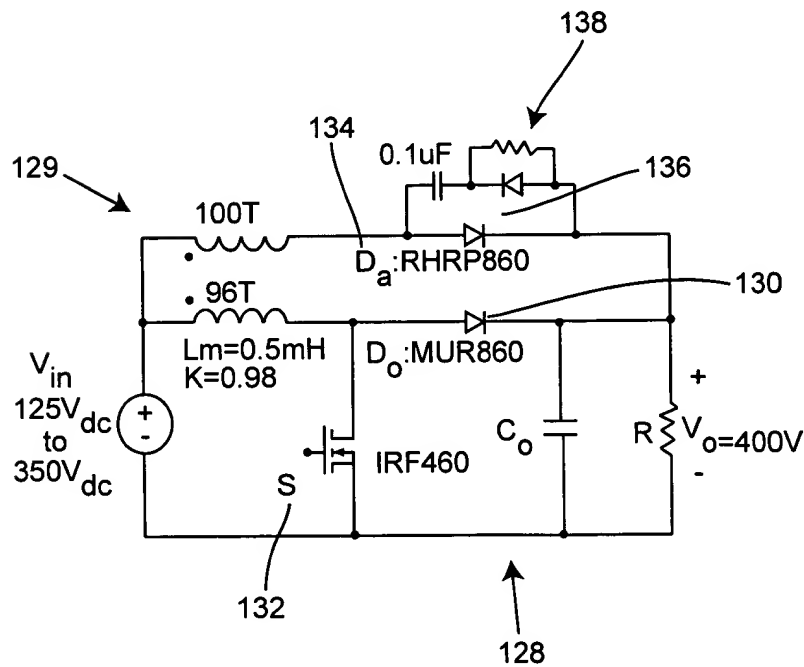


Figure 8



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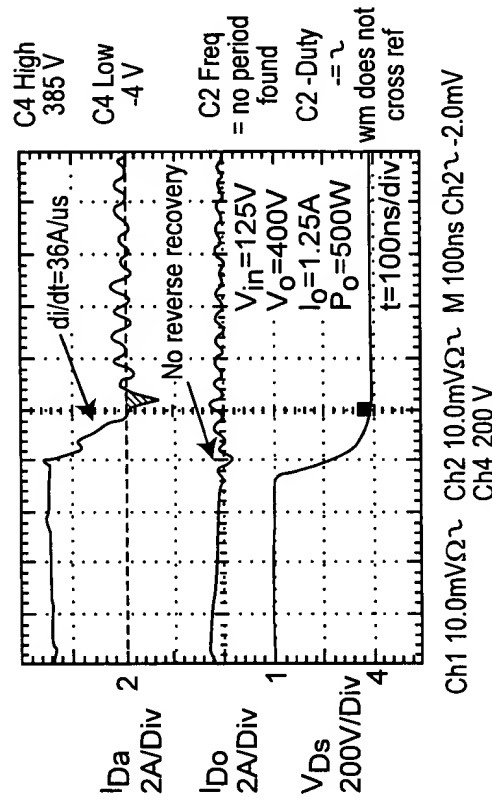


Figure 9B

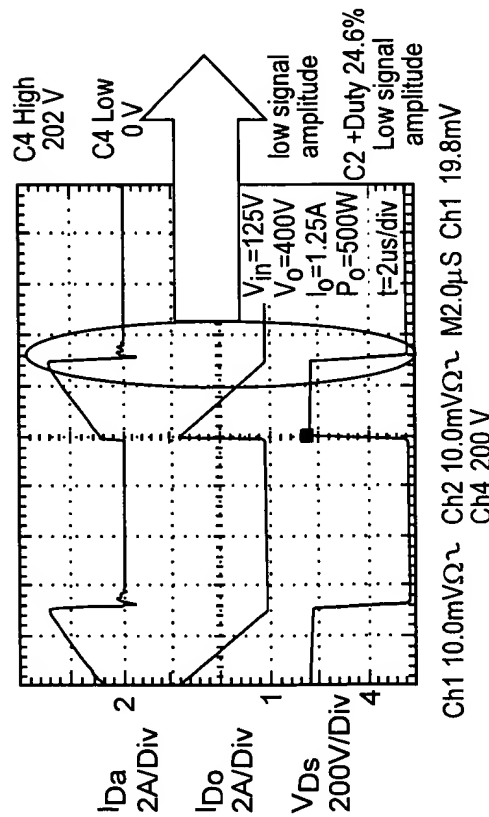


Figure 9A



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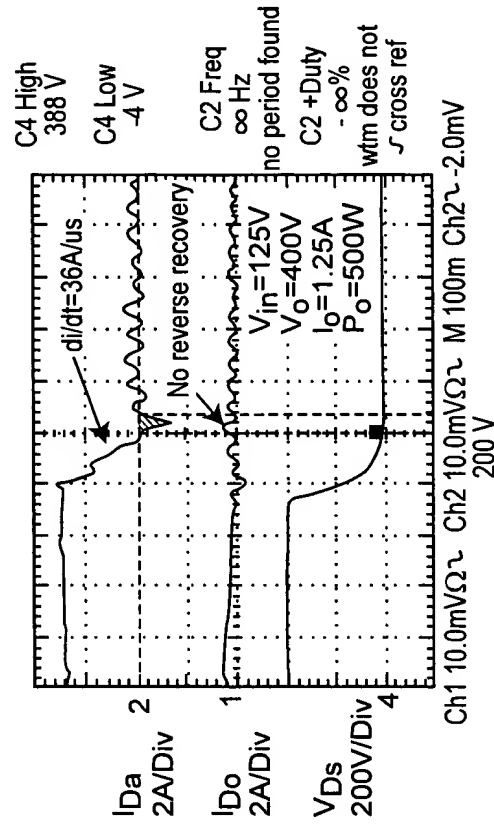


Figure 10B

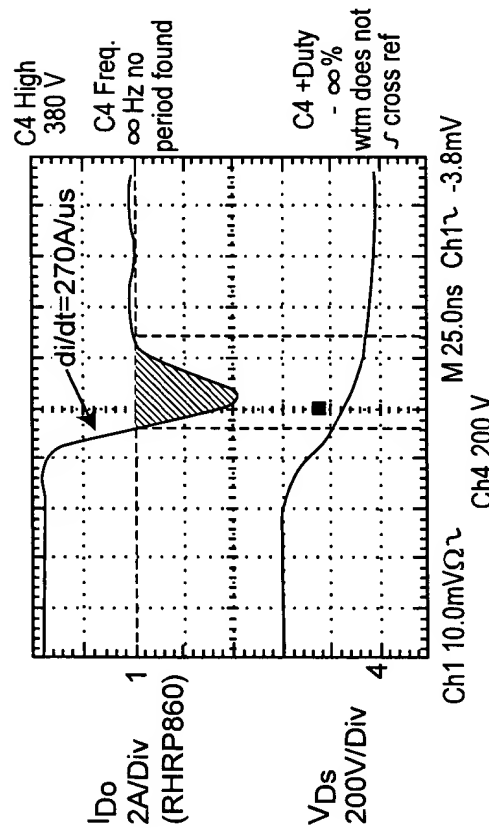


Figure 10A
(PRIOR ART)



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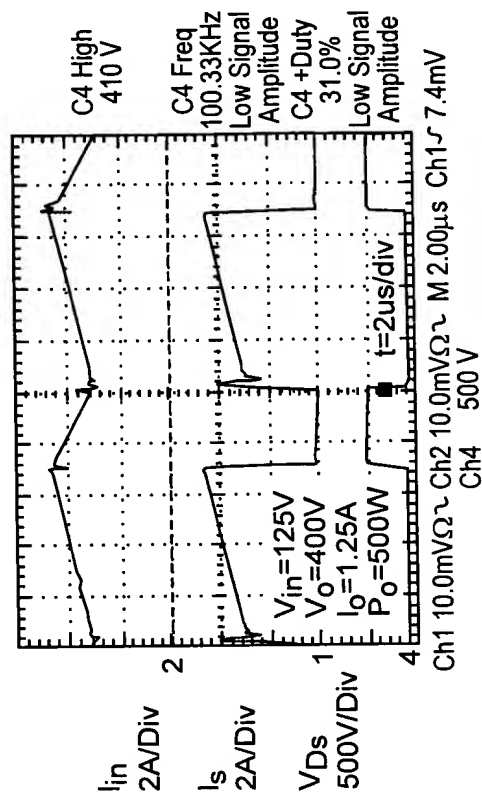


Figure 12

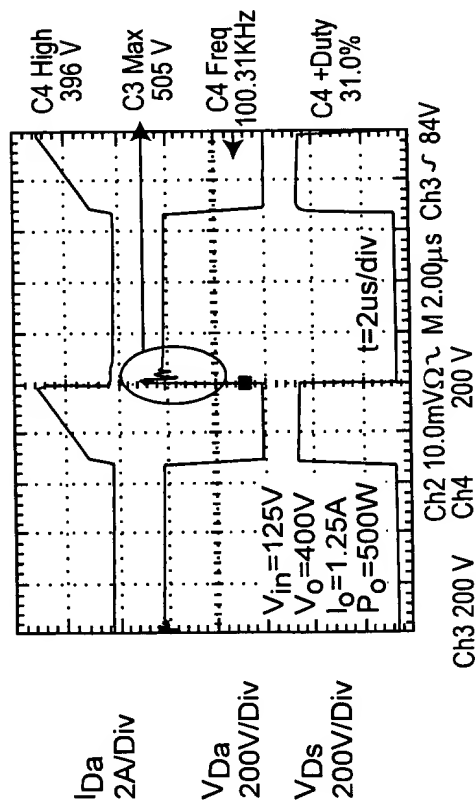
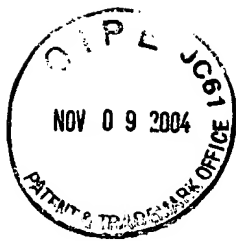


Figure 11



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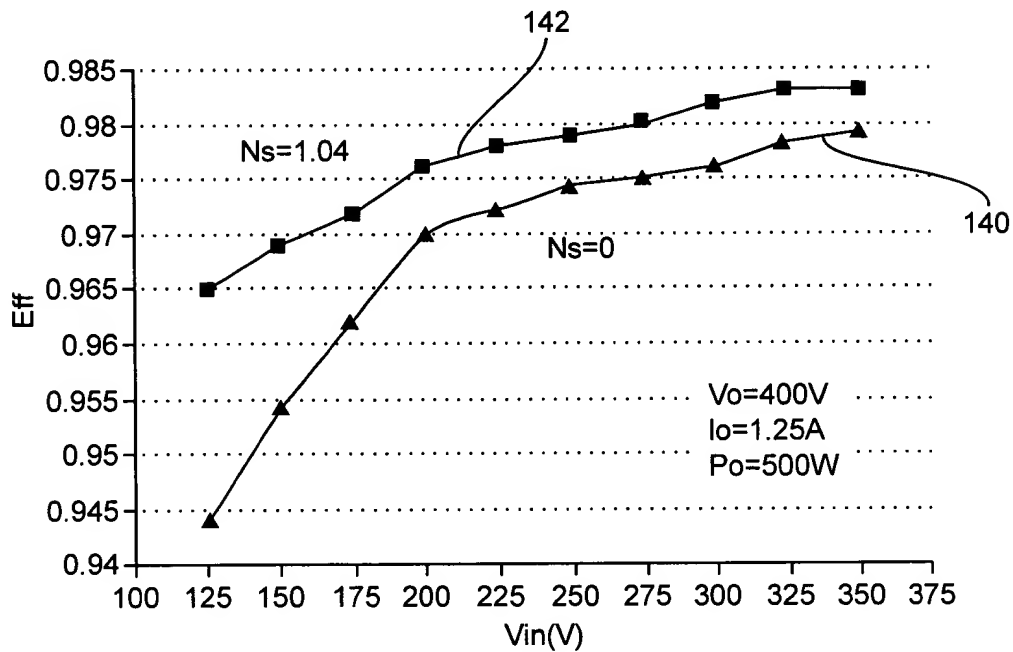


Figure 13

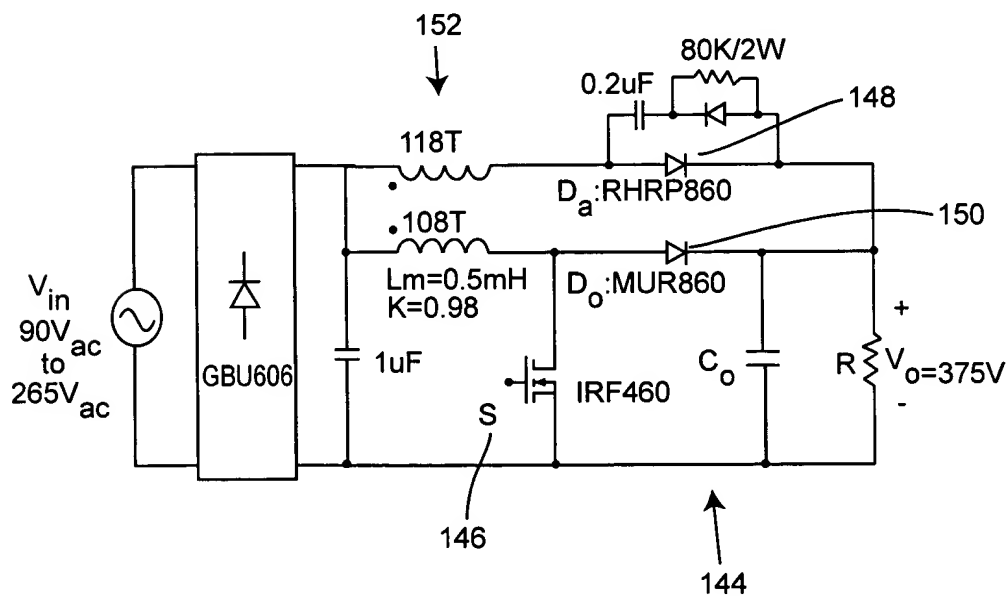
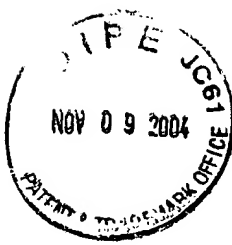


Figure 14



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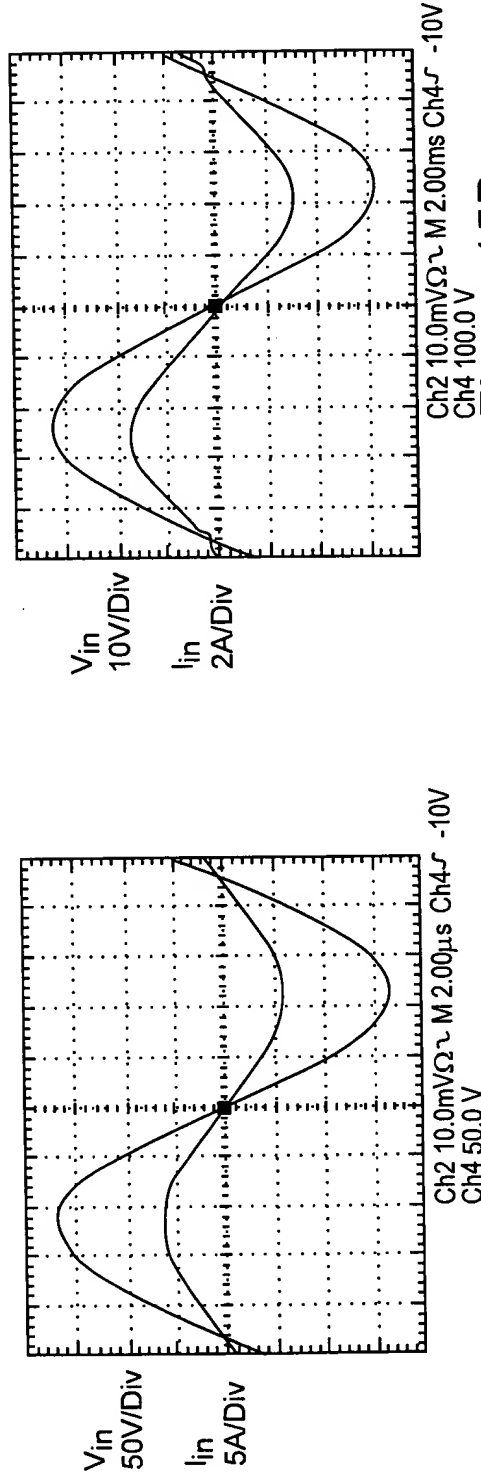


Figure 15A

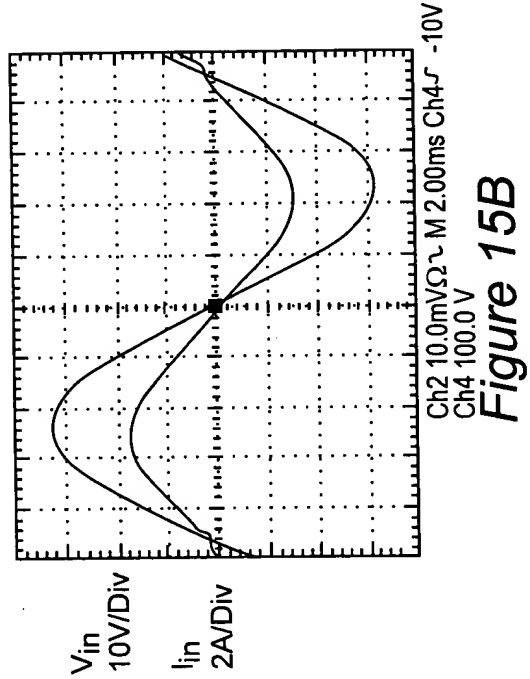


Figure 15B

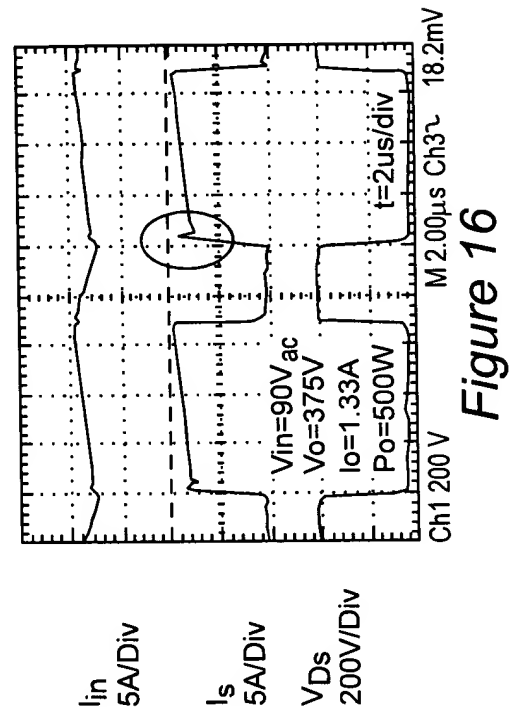


Figure 16



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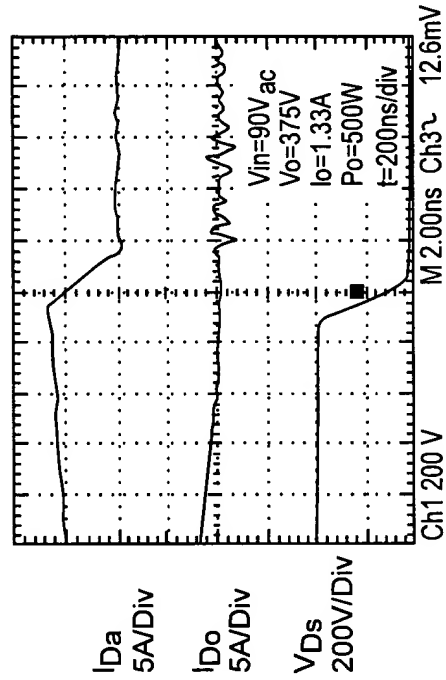


Figure 17B

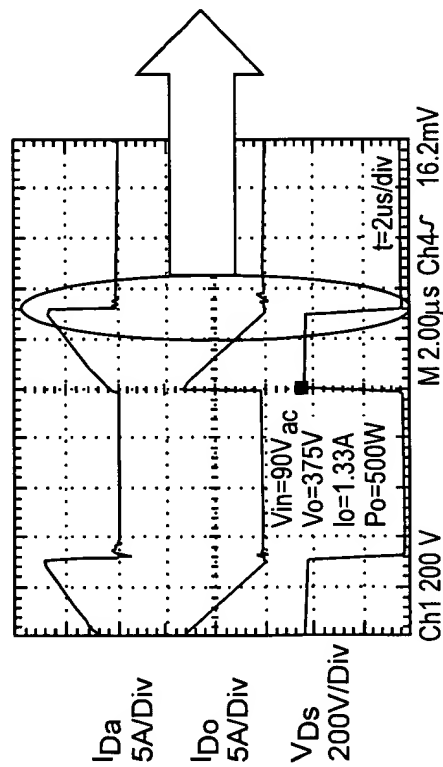


Figure 17A



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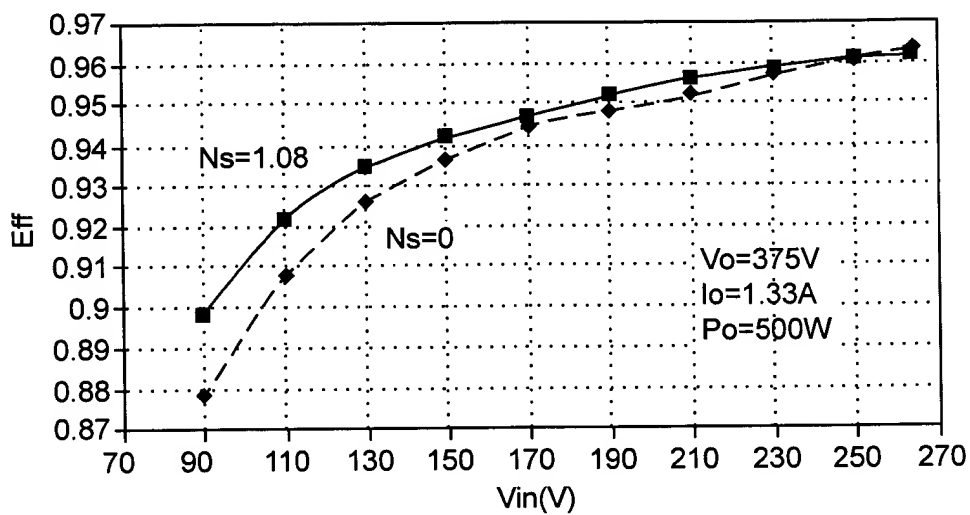


Figure 18

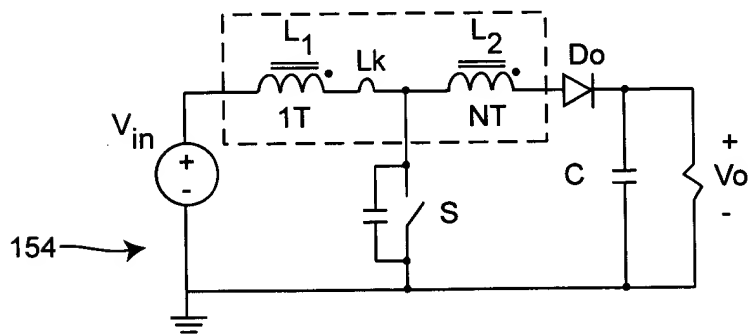


Figure 19
(PRIOR ART)

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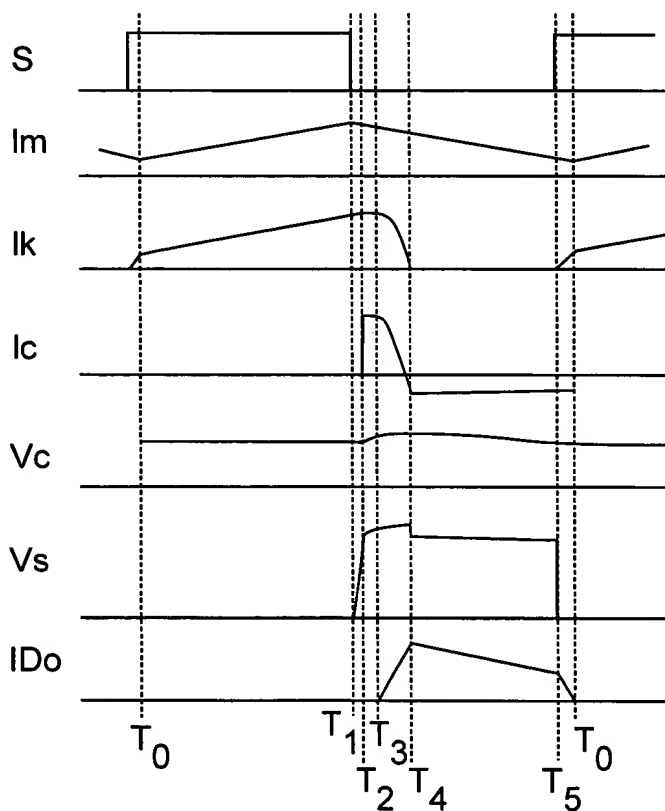
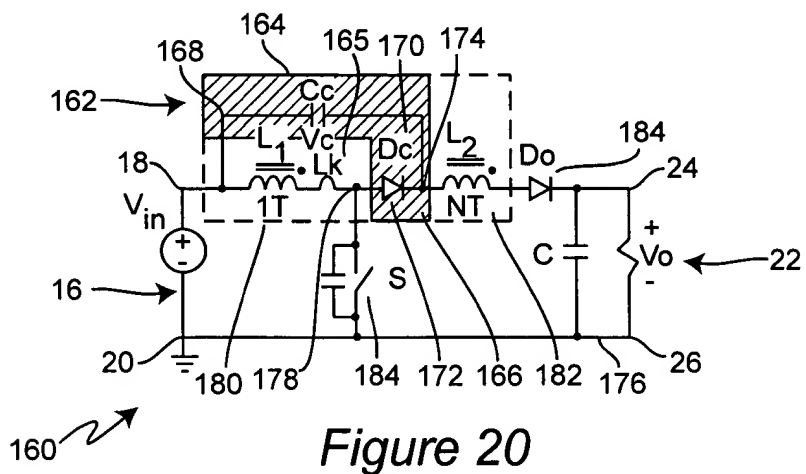


Figure 21



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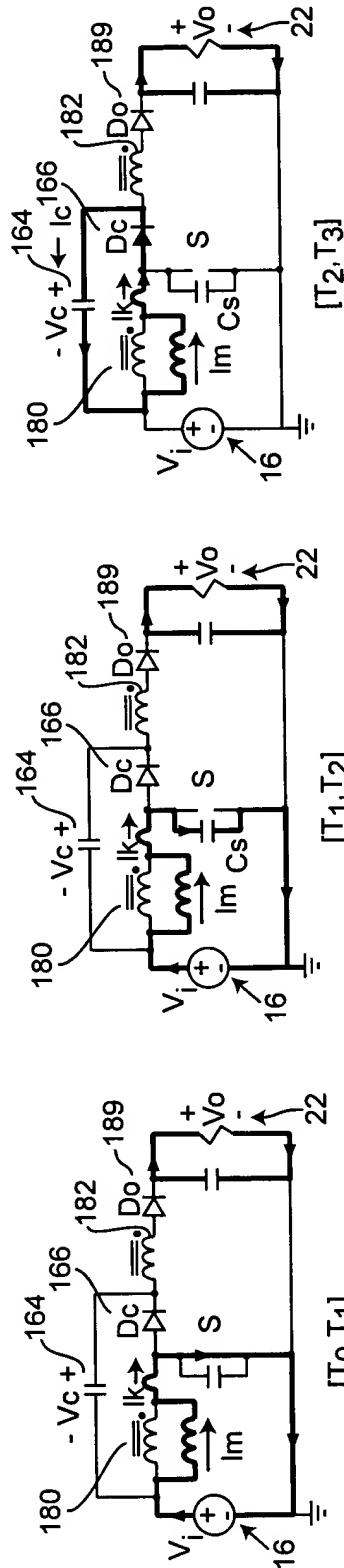


Figure 22A

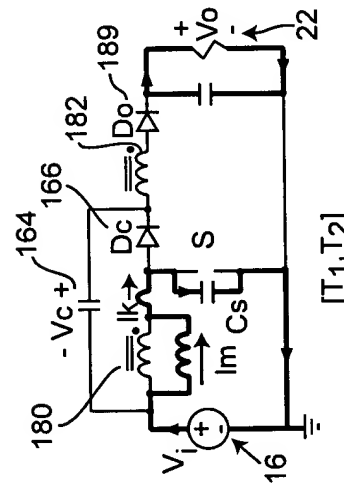


Figure 22B

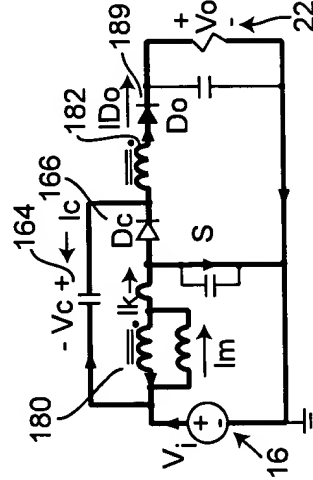


Figure 22C

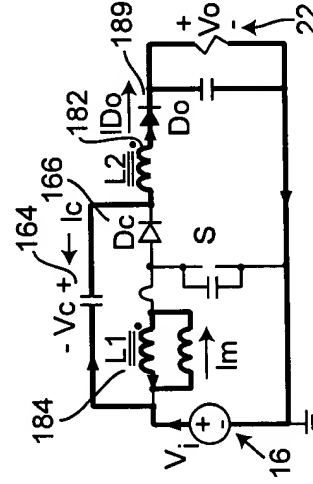


Figure 22D

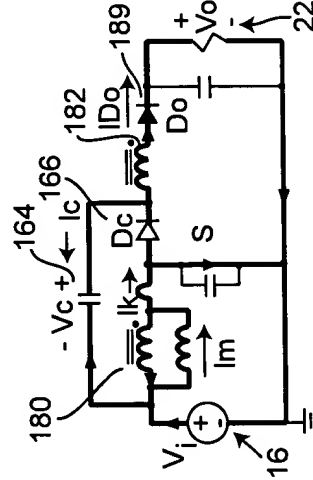


Figure 22E

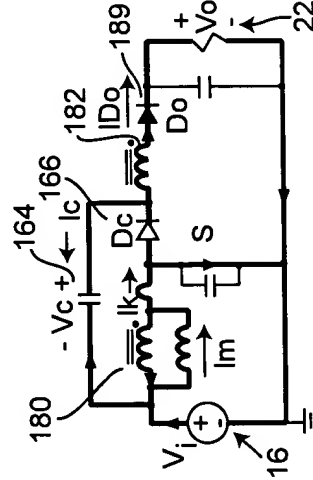


Figure 22F



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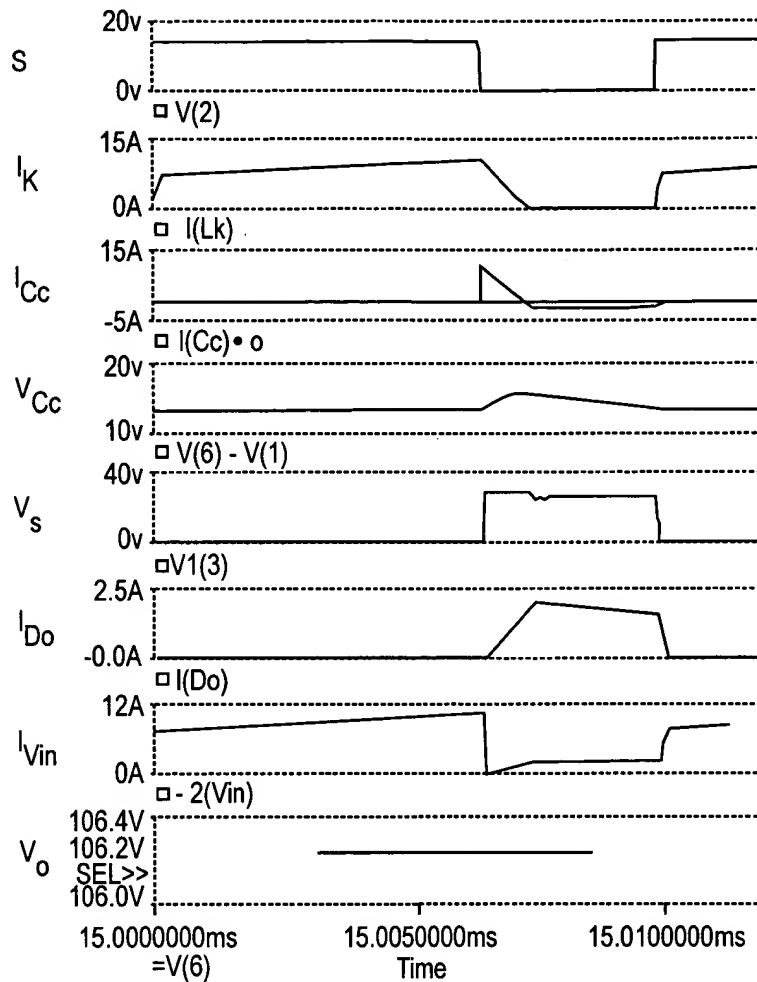
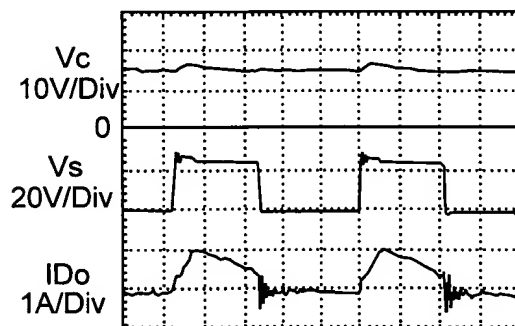


Figure 23



Vin=12V, Vo=100V, Po=35W, Fs=105Khz

Figure 24



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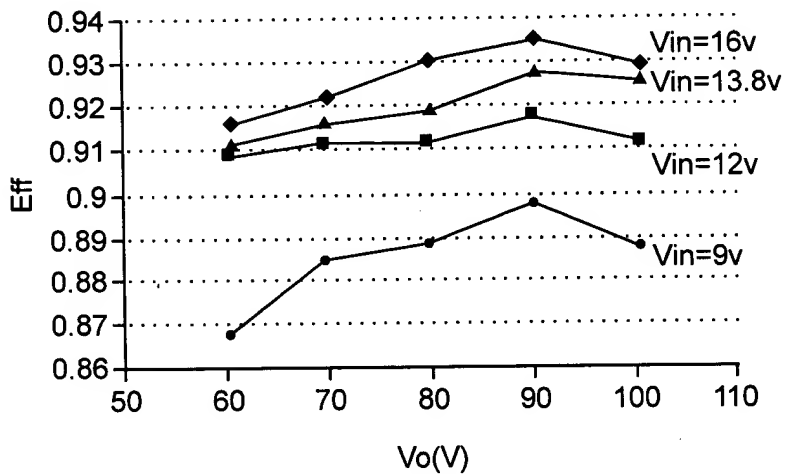


Figure 25

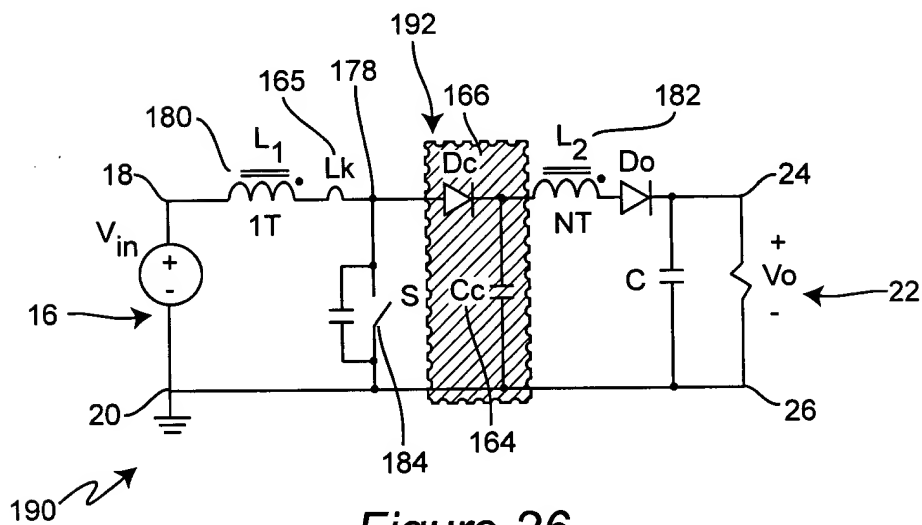
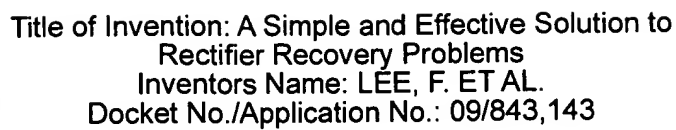


Figure 26



The circuit diagram shows a power MOSFET switching a primary winding of a transformer. The primary winding has inductance L_m and current i_m . The secondary winding has inductance L_k and current i_k , with a turns ratio of $1T$. The MOSFET gate is driven by a pulse-width modulated signal S . The secondary winding is connected to a diode D_o in series with an inductor nT . The output filter consists of a capacitor C_o and a load resistor R in parallel. The output current is I_{D_o} . The input voltage is V_{in} .

Figure 28



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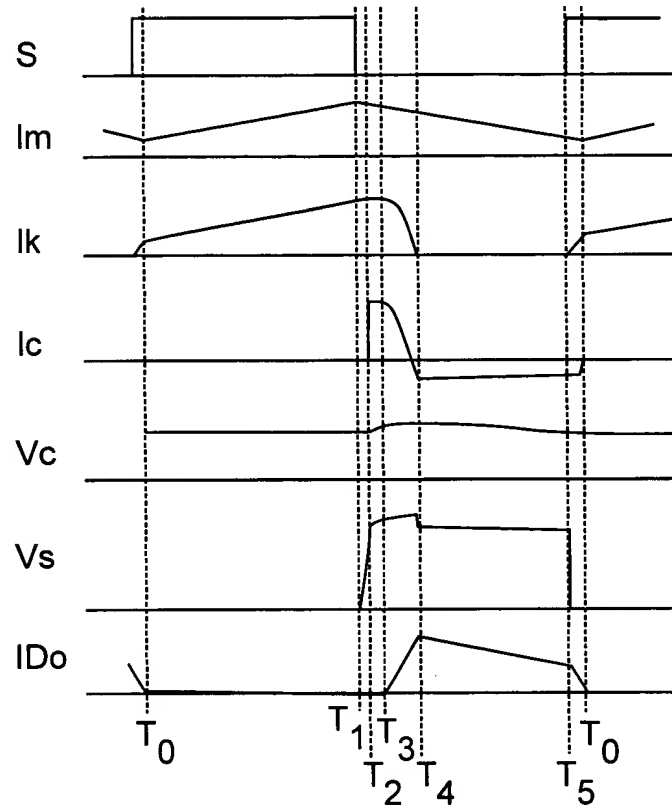
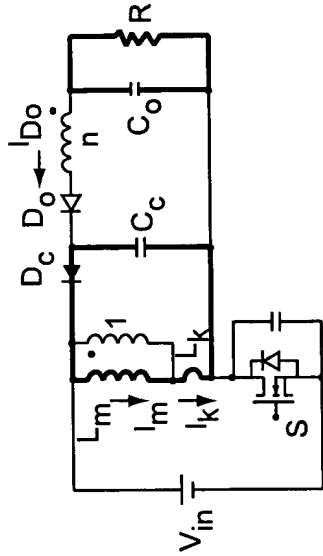


Figure 29



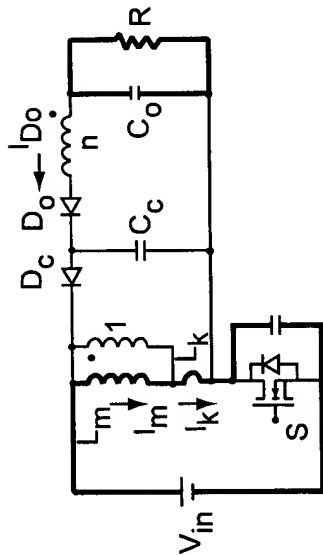
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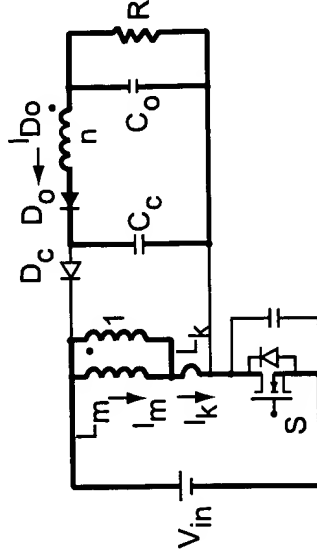
[T₀, T₁]

Figure 30A



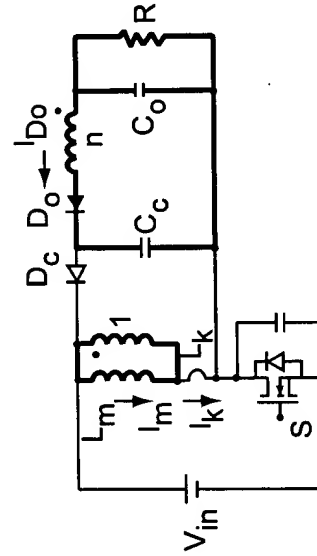
[T₁, T₂]

Figure 30B



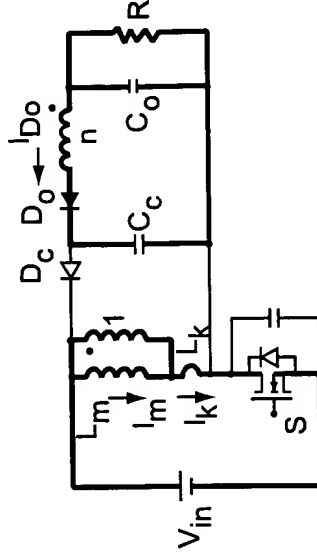
[T₂, T₃]

Figure 30C



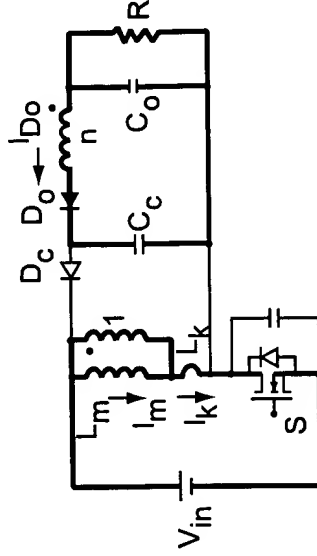
[T₃, T₄]

Figure 30D



[T₄, T₅]

Figure 30E



[T₅, T₀]

Figure 30F



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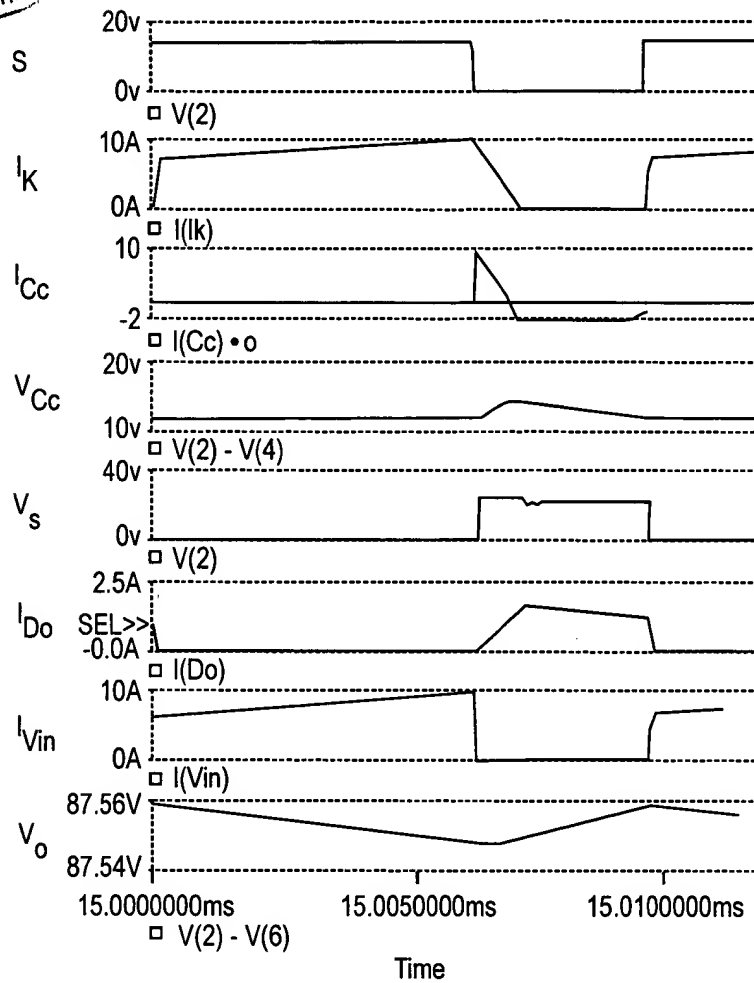


Figure 31

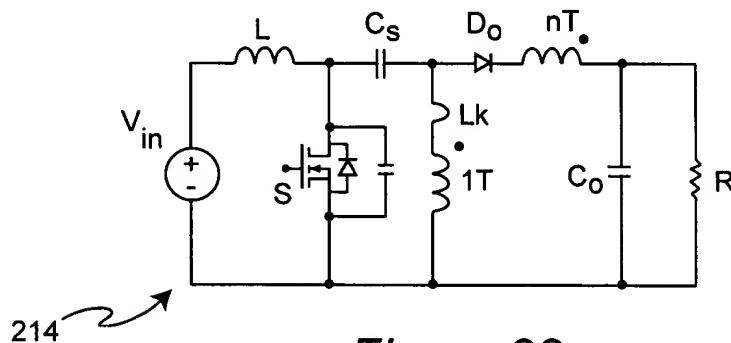


Figure 32



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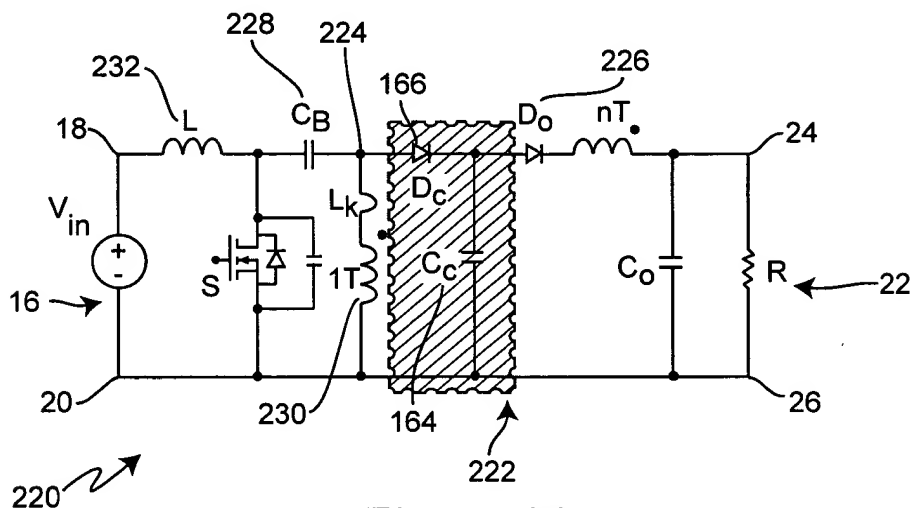


Figure 33

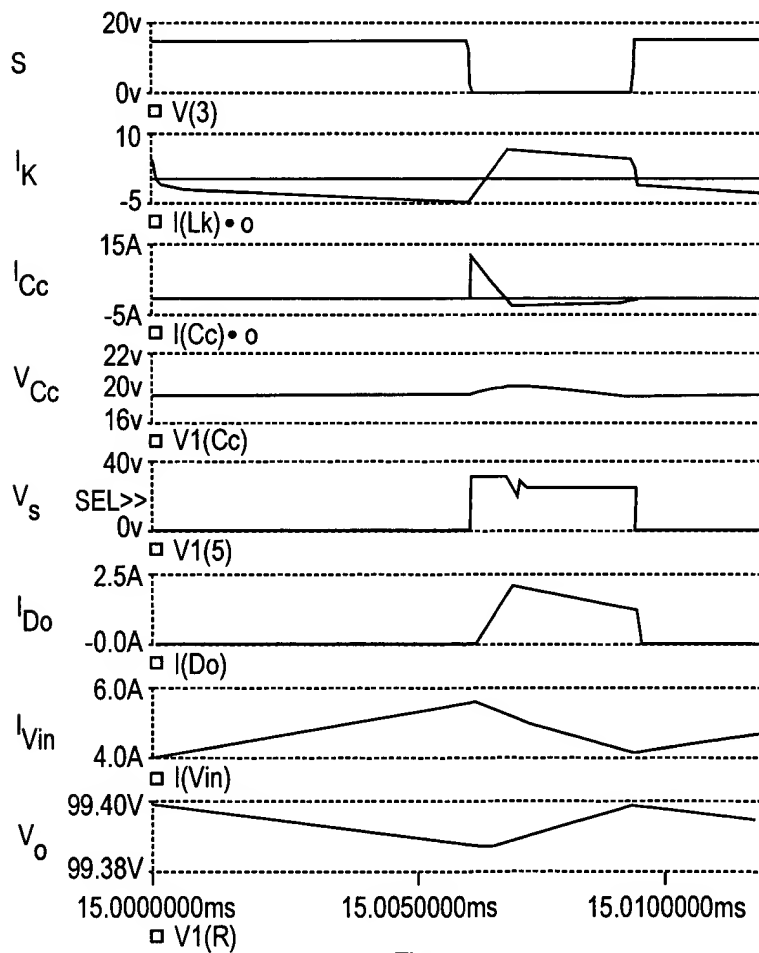


Figure 34